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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/037,361	BYRD, JAMES M.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

1. Applicant's request for reconsideration filed on 11/1/2004 has been reviewed.

2. Amendment filed on 11/1/2004 has been entered.

3. Applicant's arguments filed on 11/1/2004 have been fully considered but they are not deemed to be persuasive.

Oath/Declaration

4. A new oath or declaration is required because the priority claim to provisional application 60/286,407 is incorrect as per the Amendment filed on 11/1/2004. The wording of an oath or declaration cannot be amended. If the wording is not correct or if all of the required affirmations have not been made or if it has not been properly subscribed to, a new oath or declaration is required. The new oath or declaration must properly identify the application of which it is to form a part, preferably by application number and filing date in the body of the oath or declaration. See MPEP §§ 602.01 and 602.02.

Specification

5. The disclosure is objected to because of the following informalities:

The following corrections were not made in the amendment:

- On page 20, line 8, "Tester 300" is incorrect. It should be –Tester 200--.

The following incorrect changes were made in the amendment:

- On page 20, line 6, "Tester 300" is incorrect. It should be –Tester 200—as per the original specification.

Appropriate correction is required.

Claim Objections

6. Claim 1 is objected to because of the following informalities: Line 8 of claim 1, "an different logical value" is incorrect. It should be --a different logical value--. Appropriate correction is required.

7. Claim 13 is objected to because of the following informalities: Line 8 of claim 13, "an different logical value" is incorrect. It should be --a different logical value--. Appropriate correction is required.

Response to Arguments

8. Regarding claim 1, the applicant contends, "Kurihara does not teach shifting a first bit having a different logical value across the initial data bit combination, wherein each time the bit is shifted, one of n data bit combinations is generated. Kurihara fails to teach providing each of the n data bit combinations to the error detection/correction logic; in response to said providing, the error detection/correction logic generating a set of check bits for each of the n data bit combinations".

The examiner disagrees and asserts that Kurihara teaches an error detection circuit which comprises a shift register having a plurality of storing stages which sequentially shifts input data (col. 1, lines 44-47, Kurihara). Kurihara teaches that considering FIG. 2, the output from each stage of the shift register 101 is supplied to the parity generator 4, and a parity signal PARITY 1 is derived therefrom (figure 2, col. 3, lines 66-68, Kurihara).

- The applicant contends, "Kurihara does not teach comparing the set of check bits generated by the error correction/detection logic with a known correct set of check bits for each of the n data bit combinations".

The examiner disagrees and asserts that Kurihara teaches comparing the predicted value with the value actually generated from the error correction circuit, in order to detect malfunction of the error detection circuit (figure 1, 2, col. 2, lines 65-68, Kurihara). Kurihara teaches that a parity predictive value of the shift register portion 1 of the nth term is calculated with the count values of the counters 3 and 2 and the zeroth Po of a polynomial register, and the parity prediction value is compared with the actual parity value applied from the parity generator 4 to the check circuit 5. In the case where the values are not coincident with each other, an error signal is produced to take proper steps (figure 2, col. 3, lines 27-34, Kurihara).

- The applicant contends, "Kurihara is silent regarding the error detection/correction logic generating a set of check bits".

The examiner disagrees and asserts that Kurihara teaches an error detection circuit checking system for checking error detection within a data processing circuit (col. 4, lines 50-52, Kurihara). Kurihara teaches means for comparing the parity signal derived by the parity generator with the predictive parity signal from

the predictive parity signal generator to detect malfunction of the error detection circuit (col. 4, lines 65-68, Kurihara).

9. Regarding claim 24, the applicant contends, "Kurihara fails to teach test check bit generating means for creating a set of test data bit combinations and providing the set of test data bit combinations to a check bit generator comprised in the error correction/detection logic".

The examiner disagrees and asserts that Kurihara teaches an error detection circuit including a shift register having a plurality of storing stages for sequentially receiving input data shifted thereto and having an output stage for feeding back output data from the output stage to selected ones of the storing stages, and a parity generator for generating a parity signal in accordance with the data storing state of the storing stages of the shift register (col. 5, lines 9-16, Kurihara).

- The applicant contends, "Kurihara also fails to disclose wherein the set of test data bit combinations comprises n n-bit data bit combinations, wherein each possible value of each data bit is present in at least one of the n n-bit data bit combinations in the set of test data bit combinations. Kurihara fails to teach comparison means for comparing check bits output by the error/detection logic for each of the n n-bit data bit combinations in the set of test data bit combinations to known correct check bits for each of the n n-bit data bit combinations."

The examiner disagrees and asserts that Kurihara teaches that a parity predictive value of the shift register portion 1 of the nth term is calculated with the count values of the counters 3 and 2 and the zeroth Po of a polynomial register, and the parity prediction value is compared with the actual parity value applied from the parity generator 4 to the check circuit 5. In the case where the values are not coincident with each other, an error signal is produced to take proper steps (figure 2, col. 3, lines 27-34, Kurihara).

10. Regarding claim 27, the applicant contends, "Kurihara fails to teach a method including providing a set of m+1 test code words to the error correction/detection logic".

The examiner disagrees and asserts that Kurihara teaches an error detection circuit which comprises a shift register having a plurality of storing stages which sequentially shifts input data and feeds back output data from an output stage to desired ones of the stages, and a parity generator, and in which a parity signal is generated from the parity generator in accordance with the data storing state of the shift register

(figure 2, col. 1, lines 44-51, Kurihara). The examiner would like to point out that the input data and the shift register provides the test code words to the error correction/detection logic.

11. Regarding claim 30, the applicant contends, "Arroyo does not teach a method including providing a set of test code words to the error correction/detection logic, wherein said providing comprises introducing an error into each of the test code words in the set by substituting check bits corresponding to an unused syndrome for a correct set of check bits within each test code word, wherein each test code word comprises substituted check bits corresponding to a different unused syndrome than each other test code word in the set of test code words".

The examiner disagrees and asserts that Arroyo teaches that an error detection and correction circuit is also provided that periodically checks and corrects bit errors in the data words (col. 1, lines 36-38, Arroyo). Arroyo teaches that these ECC check bits corresponding to the generated data are then written to memory 5 from bus 4. Thus, at step 4, the actual test data from CPU 1 is written to memory 5 along with corresponding ECC check bits generated by logic 31. The 64 bit data and 8 bit ECC check bits are then read from the verified section of memory 5 at step 5. At this time, the 8 bit logical zeros are forced through enabled multiplexer 43 and to comparator 45. Additionally, logic 41 generates ECC check bits based on the actual data, which is being read from memory 5 on bus 10. Therefore, the ECC check bits actually corresponding to data on bus 10 and the 8 bit logical zero check bits are both provided to comparator 45 which then performs a comparison and generates a syndrome, at step 6. Additionally, at step 6, the status and address registers are written with the type of error, syndrome and location of the error. It can be seen that an error will in fact occur because the check bits generated by logic 41 are based upon actual data while 8 bits of logical zeros have been substituted for the check bits generated by logic 31 and input to comparator 45. At step 7 it is then determined if a single bit error has occurred and if so the process continues to step 8 where logic 47 receives the check bits (col. 7, lines 22-44, Arroyo).

12. Regarding claim 35, Kurihara in view of Arroyo fails to teach providing a subset of possible data bit combinations of n data bits to the error detection/correction logic, wherein the subset comprises n data bit combinations, wherein each possible value of each data bit is present in at least one of the n data bit combinations in the subset.

The examiner disagrees and asserts that Kurihara teaches an error detection circuit which comprises a shift register having a plurality of storing stages which sequentially shifts input data and feeds back output data from an output stage to desired ones of the stages, and a parity generator, and in which a parity signal is generated from the parity generator in accordance with the data storing state of the shift register (figure 2, col. 1, lines 44-51, Kurihara). Kurihara also teaches an error detection circuit ... logical "0" (col. 4, line 49 to col. 5, line 6, Kurihara). The examiner would like to point out that the input data and the shift register provides the n data bit combinations to the error correction/detection logic.

- The applicant contends, "Kurihara in view of Arroyo also fails to teach verifying the error detection/correction logic by comparing a set of check bits generated by the error detection/correction logic for each of the n data bit combinations in the subset with a set of known correct check bits".

The examiner disagrees and asserts that Kurihara teaches comparing the predicted value with the value actually generated from the error correction circuit, in order to detect malfunction of the error detection circuit (figure 1, 2, col. 2, lines 65-68, Kurihara). Kurihara teaches that a parity predictive value of the shift register portion 1 of the nth term is calculated with the count values of the counters 3 and 2 and the zeroth Po of a polynomial register, and the parity prediction value is compared with the actual parity value applied from the parity generator 4 to the check circuit 5. In the case where the values are not coincident with each other, an error signal is produced to take proper steps (figure 2, col. 3, lines 27-34, Kurihara).

- The applicant contends, "Kurihara in view of Arroyo also fails to teach providing a first set of m+1 test code words to the error detection/correction logic, wherein a first test code word is a correct test code word and where each other test code word in the set of m+1 test code words comprises a single-bit error, wherein each test code word having a single-bit error has the single-bit error at a different bit position than each other test code word that has a single-bit error".

The examiner disagrees and asserts that Arroyo teaches that an error detection and correction circuit is also provided that periodically checks and corrects bit errors in the data words (col. 1, lines 36-38, Arroyo). Arroyo also teaches that in the event that an error condition for a single bit data error is detected, the ECC correction logic is utilized to correct the invalid data bit (col. 1, lines 25-27, Arroyo). Arroyo

teaches that at step 14 it is then determined if each data address in the verified memory section has been tested. Different data addresses are used in the present invention so that all of the ECC logic in memory control chip 3 is tested. If the test is not complete, the process continues to step 15 wherein the CPU increments the data value by walking a bit through each position, thereby changing the ECC code generated by logic 31. The process then returns to step 5. Once all of the memory section is tested, the multiplexer 33 is disabled at step 15a (col. 6, line 61 to col. 7, line 3, Arroyo).

- The applicant contends, "Kurihara in view of Arroyo also fails to teach providing a second set of test code words to the error detection/correction logic, wherein each test code word in the second set comprises an error introduced by substituting check bits corresponding to an unused syndrome for a correct set of check bits within a correct code word, wherein each test code word in the second set comprises substituted check bits corresponding to a different unused syndrome than each other test code word in the second set of test code words.

The examiner disagrees and asserts that Arroyo teaches that an error detection and correction circuit is also provided that periodically checks and corrects bit errors in the data words (col. 1, lines 36-38, Arroyo). Arroyo teaches that these ECC check bits corresponding to the generated data are then written to memory 5 from bus 4. Thus, at step 4, the actual test data from CPU 1 is written to memory 5 along with corresponding ECC check bits generated by logic 31. The 64 bit data and 8 bit ECC check bits are then read from the verified section of memory 5 at step 5. At this time, the 8 bit logical zeros are forced through enabled multiplexer 43 and to comparator 45. Additionally, logic 41 generates ECC check bits based on the actual data, which is being read from memory 5 on bus 10. Therefore, the ECC check bits actually corresponding to data on bus 10 and the 8 bit logical zero check bits are both provided to comparator 45 which then performs a comparison and generates a syndrome, at step 6. Additionally, at step 6, the status and address registers are written with the type of error, syndrome and location of the error. It can be seen that an error will in fact occur because the check bits generated by logic 41 are based upon actual data while 8 bits of logical zeros have been substituted for the check bits generated by logic 31 and input to comparator 45. At step 7 it is then determined if a single bit error has occurred and if so the process continues to step 8 where logic 47 receives the check bits (col. 7, lines 22-44, Arroyo).

13. Regarding claim 13, The applicant contends, "Kurihara in view of Fielder et al. fails to teach a computer readable medium comprising program instructions computer executable to: create an initial data bit combination having n bits, wherein each data bit in the initial data bit combination has a same logical value as each other data bit in the initial data bit combination; shift a first bit having an different logical value than the same logical value across the initial data bit combination, wherein each time the first bit is shifted, one of n data bit combinations is generated; provide each of the n data bit combinations to error detection/correction logic; compare a set of check bits generated by the error correction/detection logic with a known correct set of check bits for each of the n data bit combinations; and dependent on an outcome of said comparing, generate an indication of whether the error detection/correction logic correctly generated the set of check bits".

The examiner would like to point out that the remarks above regarding claim 1 in view of Kurihara also apply here to claim 13.

Additionally the applicant contends, "Fielder et al. reference is not analogous art".

The examiner disagrees and asserts that Fielder et al. art teach a program of instructions executable by a machine, such as a programmable digital signal processor or computer processor, to perform such a process can be conveyed by a medium readable by the machine, and the machine can read the medium to obtain the program and responsive thereto perform such process (col. 4, lines 60-64, Fielder et al.). Fielder et al. also teach that preferred embodiments use program-controlled processors, such as those in the DSP563xx line of digital signal processors from Motorola. Programs for such implementations may include instructions conveyed by machine readable media, such as, baseband or modulated communication paths and storage media (col. 3, lines 4-9, Fielder et al.). Fielder et al. teach that a processing system for a standard data channel includes a memory unit and a program-controlled processor (col. 3, lines 52-54, Fielder et al.).

Hence, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kurihara's patent with the teachings of Fielder et al. by including an additional step of using a computer readable medium comprising program instructions that are computer-executable.

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 1, 3-5, 24, 25, 27-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurihara (US 4,107,649). Please see the office action mailed on 07/28/2004 for details.

16. Claim 30 is rejected under 35 U.S.C. 102(b) as being anticipated by Arroyo et al. (US 5,502,732). Arroyo et al. anticipate claim 30. Please see the office action mailed on 07/28/2004 for details.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

19. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (US 4,107,649) in view of Nielson et al. (US 5,619,642). Please see the office action mailed on 07/28/2004 for details.

20. Claims 6-12, 26, 31-33, 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (US 4,107,649) as applied to claim 3 above, and further in view of Arroyo et al. (US 5,502,732). Please see the office action mailed on 07/28/2004 for details.

21. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (US 4,107,649) in view of Fielder et al. (US 6,446,037 B1). Please see the office action mailed on 07/28/2004 for details.

22. Claims 17-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (US 4,107,649) and Fielder et al. (US 6,446,037 B1) as applied to claim 14 above, and further in view of Arroyo et al. (US 5,502,732). Please see the office action mailed on 07/28/2004 for details.

23. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara (US 4,107,649) in view of Vishlitzky et al. (US 5,809,332).

As per claim 34, Kurihara teaches error correction/detection logic configured to generate check bits for the data being provided to the storage array; wherein the host computer system is configured to test the error correction/detection logic by providing each of a set of n data bit combinations to the error detection/correction logic, wherein each data bit combination has n bits, wherein each possible value of each data bit is present in at least one of the n data bit combinations, wherein the set of n data bit combinations provided to the error detection/correction logic is a subset of a set of all data bit combinations that it is possible to create using n bits; wherein in response to being provided with the set of n data bit combinations, the error detection/correction logic is configured to generate a set of check bits for each of the n data bit combinations; and wherein the host computer system is configured to compare the set of check bits generated by the error correction/detection logic with a known correct set of check bits for each of the n data bit combinations (col. 3, lines 13-24, col. 5, line 52 - col. 6, line 14, Kurihara). However Kurihara does not explicitly teach the specific use of a data processing system comprising: a storage array comprising at least one mass storage device; a host computer system coupled to provide data to the storage array.

Vishlitzky et al. in an analogous art teach that such a mass storage system features a mass storage array having a plurality of mass storage devices, such as disk drives; a storage controller for receiving and sending data from and to the storage devices; a host computer connected to a standard based communications bus for communicating data and commands with the storage controller (figure 1, col. 1, lines 51-56, Vishlitzky et al.).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kurihara's patent with the teachings of Vishlitzky et al. by including an additional step of using a data processing system comprising: a storage array comprising at least one mass storage device; a host computer system coupled to provide data to the storage array.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to test the error correction/detection logic using the data stored in the storage array.

Conclusion

24. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner

Gregory J. Lamarre
Primary Examiner